IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Mikko WALTARI
Serial No: 10/749,571
Confirmation No. 8970
Filed: December 31, 2003
For: Architecture for an Algorithmic Analog-to-Digital Converter

Art Unit: 2819
Examiner: Wamsley, Patrick G

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
January 20, 2006
Date of Deposit
Juanita Soberanis
Name
Juanita Soberanis 1/20/06
Signature Date

DECLARATION UNDER 37 CFR 1.131

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Mikko Waltari, of San Diego, California, declare that:

1. I am the named inventor of the captioned U.S. application.

2. I am informed that U.S. patent 6,909,393 having a filing date of July 30, 2003 was cited in an Office Action in the captioned U.S application, and relied on in rejecting the pending claims of the application.

3. The invention claimed in the captioned U.S. application was described in my Innovation Disclosure Document dated April 4, 2003, a copy of which is attached to this declaration. As such, the invention thereof was complete at least by the date of April 4, 2003, which is a date earlier than the filing date of U.S. patent 6,909,393.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false

statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Date: 1/18/2006

Mikko Waltari

CONEXANT

Docket No.: 03CXT0011D
Ranking: Approved to File

1. Title of Innovation

An Improved Architecture for an Algorithmic Analog-to-Digital Converter

2. Division/platform Information

Digital Infotainment Division

3. Innovator(s)

Name	Innovator Information	
Mikko Waltari	Personal Information : Home Address : 4671 Torrey Circle State : CA Phone : 8583611529 Country of Domicile : US Conexant Contact Information : Address : 9868 Scranton Road, State : CA Phone : 858-713-3612 Email : mikko.waltari@conexant.com Mail Code : SA3-370	City : San Diego Zip : 92130 Fax : Citizenship : US City : San Diego Zip : 92121-1762 Fax : Dept. : 039-327- Supervisor : Mr. Efram Burlingame

4. Problem Solved

This invention will be part of Tiger (CX85236), the rev A tape out of which is 06/09. The same circuitry will be later used in Mako (CX25837), the rev A tape out of which will be in mid July, and Mojo (tape out later this year). This innovation is an analog-to-digital converter (ADC). It is very area efficient, thanks to heavily serial operation principle. The new architecture is based on the well-known algorithmic (or cyclic) ADC. It can be used for resolutions from 7 to 14 bits and up to 20-50 MHz clock frequencies. For instance, video rate ADCs fall into this category.

5. Previous Solutions

The most widely used ADC architecture in this speed and resolution range is the pipeline topology. Algorithmic ADC is known to be area efficient, but it has been too slow to be used as a video ADC. The existing algorithmic ADCs consist of at least two single-bit processing units, which can share a common operational amplifier.

Prior art publications:

K. Nagaraj, ?Efficient Circuit Configurations for Algorithmic Analog to Digital Converters?, IEEE Tran. CAS-II, pp. 777-785, Dec 1993.

US patent 5,861,832, US patent 5,212,486

6. Solution

This innovation uses the algorithmic principle, but contains only one processing unit, which makes its area very small. To achieve a high conversion rate it processes multiple bits in each cycle. The processing unit, which is based on switched capacitor implementation, resembles a multi-bit stage in a pipelined ADC.

The architecture consists of a sample-and-hold (S/H) circuit and multi-bit serial A/D processing unit. These two circuits work in parallel and can share a single opamp. The S/H circuit works at sampling rate (with uneven duty cycle) while the processing unit uses N times higher frequency (N is an integer). Thus, each A/D conversion is carried out in N phases each yielding k effective bits plus one redundant bit. The redundant bit is used to perform the Redundant Sign Digit (RSD) algorithm, which corrects comparator errors. After the N cycles N*k+1 bit A/D conversion result can be formed using the sub-conversion results. This process is analogous to the one used in pipelined ADCs.

See the attached document for figures and more details.

7. Differences/Advantages Over Previous Solutions

- use of single MDAC based A/D processing unit instead of two makes the area very small.

- resolving multiple bits per conversion cycle yield certain number of bits in fewer conversion cycles resulting a higher conversion rate.

- having a S/H circuit operating in parallel with the ADC maximizes the sampling time and thus alleviates the task of the circuit providing the input signal. Maximizing the component sharing between the S/H and the ADC result small area and power consumption.

8. Status of Innovation

Under development If "Other", please specify

9. Product or program in which innovation will be used:

Products Used : Decoder	Technology Used : A/D
If other, please specify :	**If other, please specify :**
Mako, Tiger, Mojo	

Additional Information :	

10. Has anyone disclosed or does anyone plan to disclose your innovation outside the Company?

○ Yes ● No ○ Don't Know

11. Has anyone proposed or does anyone plan to propose a product or program to a customer which includes your innovation?

○ Yes ○ No ● Don't Know

12. Innovator signature(s): (Do not use black ink)

_____ **Date :** _____
(MIKKO WALTARI)

Qtr Evaluated: 3Q03
Group: Digital Infotainment Division
Technology:
Sub Technology 1:
Sub Technology 2:
Products:
Innovation Block:

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